

<b>Notice of References Cited</b>	Application/Control No. 09/914,429	Applicant(s)/Patent Under Reexamination SATO ET AL.	
	Examiner A. M. Thompson	Art Unit 2825	Page 1 of 1

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**NON-PATENT DOCUMENTS**

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	V	M. Motomura et al., An Embedded DRAM-FPGA Chip with Instantaneous Logic Reconfiguration, 1997 Symposium on VLSI Circuits, pages 55-56, June 1997.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.